WHAT IS CLAIMED IS:

1. A single electron device comprising:

a source electrode and a drain electrode of semiconductor layer, formed on a substrate, the source electrode and the drain electrode being spaced a predetermined distance apart each other;

a hemisphere-type silicon layer, as an active layer, formed between the source electrode and the drain electrode, the hemisphere-type silicon layer having a plurality of electron islands;

a gate insulating layer formed on a top surface of the entire structure; and

a gate electrode formed on the gate insulating layer in order to apply voltage to the active layer.

2. The single electron device as claimed in claim 1, wherein the predetermined distance is 100 nm or less.

3. The single electron device as claimed in claim 1, wherein the thickness of the hemisphere-type silicon layer is in the range of 3 to 5 nm, and the size of the silicon electron islands is in the range of 3 to 5 nm.

4. A method of manufacturing single electron device, the method comprising the steps of, on a substrate:

forming source/drain regions of semiconductor layer, the source

region and the drain region being spaced a predetermined distance apart each other;

defining active region between the source and the drain region by depositing an amorphous silicon layer on the semiconductor layer;

changing the amorphous silicon layer into a hemisphere-type silicon layer having a plurality of silicon electron islands;

forming a gate insulating layer on the top surface of the entire structure; and

forming a gate electrode on the gate insulating layer in order to apply voltages to the active regions.

5. The method as claimed in claim 4, wherein the step of forming the hemisphere-type silicon layer comprises steps of:

spraying a silicon contained gas for a first predetermined time while maintaining the amorphous silicon layer under the condition of a temperature of 500 to 700℃ and a high vacuum state not more than 1 to $3x10E^{-7}$ torr; and

performing heat treatment for a second predetermined time at a temperature of 500 to 700℃.

6. The method as claimed in claim 5, wherein the silicon contained gas is SiH_4 or Si_2H_6.

7. The method as claimed in claim 5, wherein the first predetermined time is in the range of 10 to 170 seconds, and the second

predetermined time is in the range of 10 to 90 seconds.

8. The method as claimed in claim 4, wherein the predetermined distance is 100 nm or less, the thickness of the hemisphere-type silicon layer is in the range of 3 to 5 nm, and the size of the silicon electron islands is in the range of 3 to 5 nm.

9. The method as claimed in claim 4, wherein the predetermined distance is 100 nm or less.

10. The method as claimed in claim 4, wherein the substrate is an SOI substrate, and the semiconductor layer is a most upper layer of the SOI substrate.

11. A method of simultaneously manufacturing a single electron device and an MOS transistor, the method comprising the steps of:

defining a single electron device region (hereinafter, A region) and an MOS transistor region (hereinafter, B region);

depositing a semiconductor layer entirely on the A region and B region;

defining a source and drain region of the single electron device in the A region, the source and the drain region of the A region being spaced a predetermined distance apart each other, and simultaneously defining a source, a drain, and an active region of the MOS transistor with one body in the B

region;

after depositing an amorphous silicon layer on the semiconductor layer, defining an active region of the single electron device between the source and drain regions on the A region;

changing the amorphous silicon layer of the A region into a hemisphere-type silicon layer having plurality of silicon electron islands;

forming a gate insulating layer on the top surface of the entire structure;

forming a gate electrode on the gate insulating layer; and

forming source/drain electrodes of the single electron device and the MOS transistor.

12. The method as claimed in claim 11, wherein the step of forming the gate insulating layer comprises steps of:

forming a first gate insulating layer on only the A region after covering the B region with photo-resist; and

forming a second gate insulating layer on the entire structure, wherein the thickness of the gate insulating layer in the A region is bigger than that of the gate insulating layer in the B region.